Software implementation of Post-Quantum Cryptography

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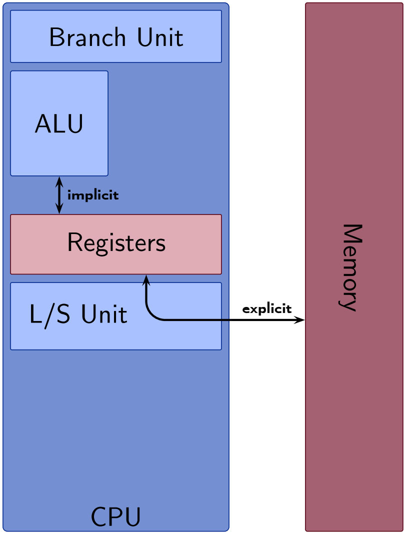
October 20, 2013

ASCrypto 2013, Florianópolis, Brazil

Part I

Optimizing cryptographic software with vector instructions

Computers and computer programs
A highly simplified view



- A program is a sequence of *instructions*
- Load/Store instructions move data between memory and registers (processed by the L/S unit)
- Branch instructions (conditionally) jump to a position in the program
- Arithmetic instructions perform simple operations on values in registers (processed by the ALU)
- Registers are fast (fixed-size) storage units, addressed "by name"

A first program
Adding up 1000 integers

1. Set register R1 to zero
2. Set register R2 to zero
3. Load 32-bits from address START+R2 into register R3
4. Add 32-bit integers in R1 and R3, write the result in R1
5. Increase value in register R2 by 4
6. Compare value in register R2 to 4000
7. Goto line 3 if R2 was smaller than 4000

A first program
Adding up 1000 integers in readable syntax

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int32 result
int32 tmp
int32 ctr

result  = 0
ctr     = 0
looptop:
tmp = mem32[START+ctr]
result += tmp
ctr += 4
unsigned<? ctr - 4000
goto looptop if unsigned<
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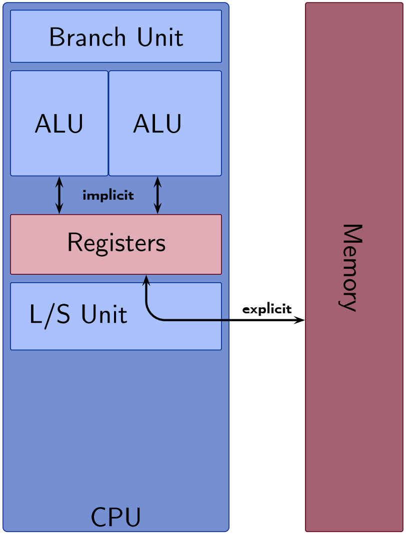
- While we're at it: Why not deploy two ALUs
- This concept is called *superscalar* execution
- Number of independent instructions of one type per cycle: **throughput**
- Number of cycles that need to pass before the result can be used: **latency**

An example computer
Still highly simplified



Latencies and throughputs

- At most 4 instructions per cycle
- At most 1 Load/Store instruction per cycle
- At most 2 arithmetic instructions per cycle
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- At least 1999 instructions: ≥ 500 cycles
- **Lower bound**: 1000 cycles

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- Total: > 8000 cycles

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- Addition has to wait for load
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- Each iteration of the loop takes 8 cycles
- Total: > 8000 cycles
- **This program sucks!**

Making the program fast

Step 1 – Unrolling

```
result  = 0
tmp = mem32[START+0]
result += tmp
tmp = mem32[START+4]
result += tmp
tmp = mem32[START+8]
result += tmp

...

tmp = mem32[START+3996]
result += tmp
```

- Remove all the loop control: *unrolling*

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- Each load-and-add now takes 3 cycles
- Total: ≈ 3000 cycles

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result += tmp
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- Remove all the loop control: *unrolling*
- Each load-and-add now takes 3 cycles
- Total: ≈ 3000 cycles
- Better, but still too slow

Making the program fast
Step 2 – Instruction Scheduling

```
result = mem32[START + 0]
tmp0   = mem32[START + 4]
tmp1   = mem32[START + 8]
tmp2   = mem32[START +12]

result += tmp0
tmp0 = mem32[START+16]
result += tmp1
tmp1 = mem32[START+20]
result += tmp2
tmp2 = mem32[START+24]

...

result += tmp2
tmp2 = mem32[START+3996]
result += tmp0
result += tmp1
result += tmp2
```

- Load values earlier
- Load latencies are hidden
- Use more registers for loaded values (`tmp0`, `tmp1`, `tmp2`)
- Get rid of one addition to zero

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- Load values earlier
- Load latencies are hidden
- Use more registers for loaded values (tmp0, tmp1, tmp2)
- Get rid of one addition to zero
- Now arithmetic latencies kick in
- Total: ≈ 2000 cycles

Making the program fast

Step 3 – More Instruction Scheduling (two accumulators)

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result0 = mem32[START + 0]
tmp0    = mem32[START + 8]
result1 = mem32[START + 4]
tmp1    = mem32[START +12]
tmp2    = mem32[START +16]

result0 += tmp0
tmp0 = mem32[START+20]
result1 += tmp1
tmp1 = mem32[START+24]
result0 += tmp2
tmp2 = mem32[START+28]

...

result0 += tmp1
tmp1 = mem32[START+3996]
result1 += tmp2
result0 += tmp0
result1 += tmp1
result0 += result1
```

- Use one more accumulator register (`result1`)
- All latencies hidden
- Total: 1004 cycles
- Asymptotically n cycles for n additions

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- Note: Good instruction scheduling typically requires more registers
- Opposing requirements to **register allocation** (assigning registers to live variables, minimizing memory access)
- Both instruction scheduling and register allocation are NP hard
- So is the joint problem
- Many instances are efficiently solvable

Architectures and microarchitectures

What instructions and how many registers do we have?

- Instructions are defined by the **instruction set**
- Supported register names are defined by the **set of architectural registers**
- Instruction set and set of architectural registers together define the **architecture**
- Examples for architectures: x86, AMD64, ARMv6, ARMv7, UltraSPARC
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What determines latencies etc?

- Different **microarchitectures** implement an architecture
- Latencies and throughputs are specific to a microarchitecture
- Example: Intel Core 2 Quad Q9550 implements the AMD64 architecture

Out-of-order execution

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- Harder to screw up completely

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- Most critical for software implementations on "large" CPUs: software must take constant time (independent of secret data)

Timing leakage part I

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- Obvious timing leak if s is secret
- Even if A and B take the same amount of cycles this is *not* constant time!
- Reason: Conditional branch takes different amount of cycles whether taken or not
- **Never use secret-data-dependent branch conditions**

Eliminating branches

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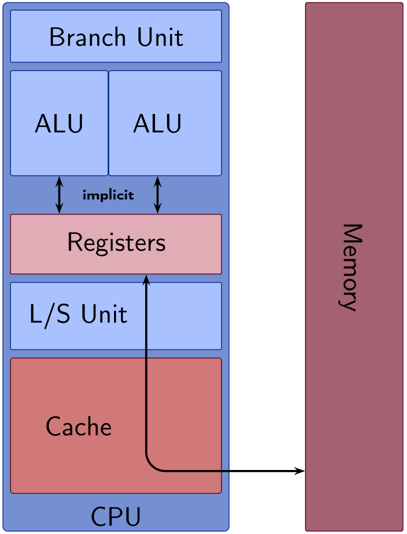
- For very fast A and B this can even be faster

Cached memory access



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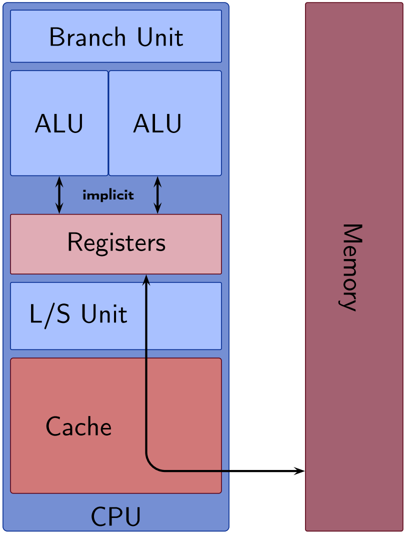

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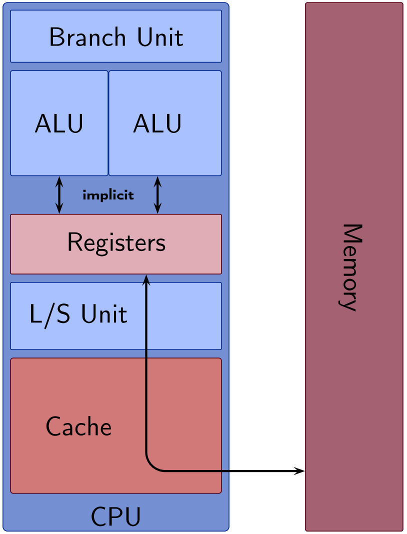

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- Loading data is fast if data is in the cache (**cache hit**)
- Loading data is slow if data is not in the cache (**cache miss**)

Timing leakage part II

$T[0] \dots T[15]$
$T[16] \dots T[31]$
$T[32] \dots T[47]$
$T[48] \dots T[63]$
$T[64] \dots T[79]$
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$T[224] \dots T[239]$
$T[240] \dots T[255]$

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- *Cache lines* have 64 bytes
- Crypto and the attacker's program run on the same CPU
- Tables are in cache

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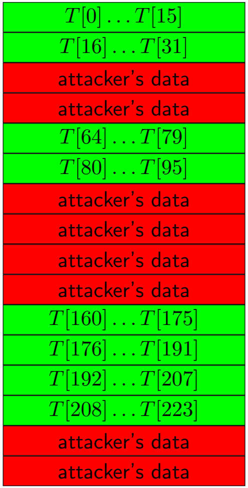

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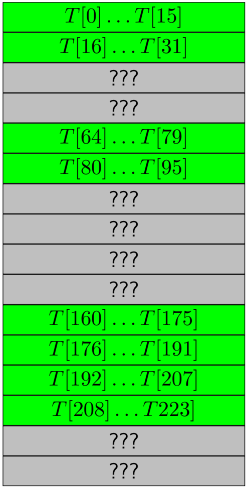

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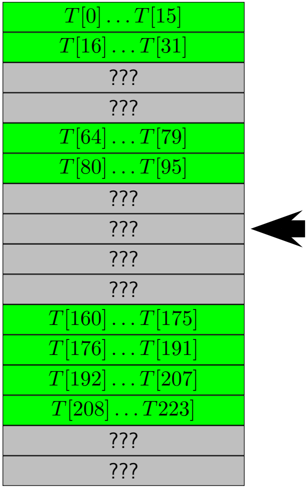

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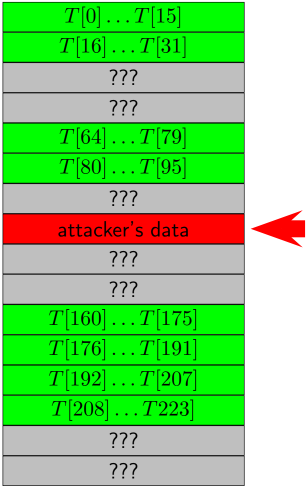

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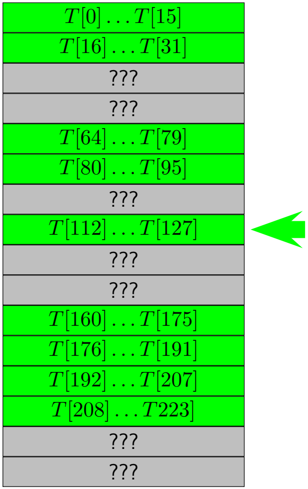

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- Attacker loads his data:
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  - Slow: cache miss (crypto just loaded from this line)

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- Load/Store addresses influence timing in many different ways
- **Do not access memory at secret-data-dependent addresses**

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- *Remote* timing attacks are practical:
  Brumley, Tuveri, 2011: A few minutes to steal ECDSA signing key from OpenSSL implementation

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- Want to load item at (secret) position p from table of size n
- Load all items, use arithmetic to pick the right one:

```
**for** $i$ from $0$ to $n-1$ **do**
    $d \leftarrow T[i]$
    **if** $p = i$ **then**
        $r \leftarrow d$
    **end if**
**end for**
```

Eliminating lookups

- Want to load item at (secret) position p from table of size n
- Load all items, use arithmetic to pick the right one:

```
for $i$ from $0$ to $n-1$ do
    $d \leftarrow T[i]$
    if $p = i$ then
        $r \leftarrow d$
    end if
end for
```

- Problem 1: if-statements are not constant time (see before)

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```

- Problem 1: if-statements are not constant time (see before)
- Problem 2: Comparisons are not constant time, replace by:

```
static unsigned long long eq(uint32_t a, uint32_t b)
{
  unsigned long long t = a ^ b;
  t = (-t) >> 63;
  return 1-t;
}
```

Timing leakage part III

- Are secret branch conditions and secret load/store addresses the only problem?

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- Some architectures have *non-constant-time* arithmetic
- Examples:
  - `UMULL`/`SMULL` and `UMLAL`/`SMLAL` on ARM Cortex-M3
  - `DIV` instruction on Intel processors, see also https://www.imperialviolet.org/2013/02/04/luckythirteen.html

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Summary

- Writing efficient constant-time code is hard
- Typically requires reconsiderations through all optimization levels

SIMD computations

"Thus we arbitrarily select a reference organization : the IBM 704-70927090. This organization is then regarded as the prototype of the class of machines which we label:
1) Single Instruction Stream–Single Data Stream (SISD).

Three additional organizational classes are evident.
2) Single Instruction Stream–Multiple Data Stream (SIMD)
3) Multiple Instruction Stream–Single Data Stream (MISD)
4) Multiple Instruction Stream–Multiple Data Stream (MIMD)"

– Michael J. Flynn. Very high-speed computing systems. 1966.

SISD

Example: 32-bit integer addition

```
int64 a
int64 b
a = mem32[addr1 + 0]
b = mem32[addr2 + 0]
(uint32) a += b
mem32[addr3 + 0] = a
```

SIMD with vector instructions

Example: 4 32-bit integer additions

```
reg128 a
reg128 b
a = mem128[addr1 + 0]
b = mem128[addr2 + 0]
4x a += b
mem128[addr3 + 0] = a
```

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  - vector addition is as fast as scalar addition
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  - vector addition is as fast as scalar addition
  - vector loads are as fast as scalar loads
- Need only 250 vector additions, 250 vector loads
- Lower bound of 250 cycles
- Very straight-forward modification of the program
- Fully unrolled loop needs only $1/4$ of the space

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  - $4\times$ 32-bit add throughput: 2 per cycle
  - 128-bit store throughput: 1 per cycle
- **Vector instructions are almost as fast as scalar instructions but do $4\times$ the work**
- Situation on other architectures/microarchitectures is similar
- Reason: cheap way to increase arithmetic throughput (less decoding, address computation, etc.)

More reasons for using vector arithmetic

- Data-dependent branches are expensive in SIMD
- Variably indexed loads (lookups) into vectors are expensive
- Need to rewrite algorithms to eliminate branches and lookups

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- Variably indexed loads (lookups) into vectors are expensive
- Need to rewrite algorithms to eliminate branches and lookups
- Secret-data-dependent branches and secret branch conditions are the major sources of timing-attack vulnerabilities
- Strong synergies between speeding up code with vector instructions and protecting code!

Vectorization problems I

Carry handling

- When adding two 32-bit integers, the result may have 33 bits (32-bit result + carry)
- Scalar additions keep the carry in a special *flag register*
- Subsequent instructions can use this flag, e.g., "add with carry"

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    - Answer 1: Special “carry generate” instruction (e.g., CBE-SPU)
    - Answer 2: They’re lost, recomputation is very expensive
- Need to *avoid carries* instead of handling them
- No problem for today’s talk, but requires care for big-integer arithmetic

Vectorization problems II

Removing instruction-level parallelism

- If we don't vectorize we perform multiple independent instructions
- We turn *data-level parallelism (DLP)* into *instruction-level parallelism (ILP)*

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- Problematic for algorithms with, e.g., 4-way DLP
- Good example to see this: ChaCha/Salsa/Blake
- Vectorization of ChaCha and Salsa can resort to higher-level parallelism (multiple blocks)
- Harder for Blake: each block depends on the previous one

Vectorization problems III

Data shuffeling

- Consider multiplication of 4-coefficient polynomials $f = f_0 + f_1x + f_2x^2 + f_3x^3$ and $g = g_0 + g_1x + g_2x^2 + g_3x^3$:

$$\begin{aligned}
r_0 &= f_0g_0 \\
r_1 &= f_0g_1 + f_1g_0 \\
r_2 &= f_0g_2 + f_1g_1 + f_2g_0 \\
r_3 &= f_0g_3 + f_1g_2 + f_2g_1 + f_3g_0 \\
r_4 &= f_1g_3 + f_2g_2 + f_3g_1 \\
r_5 &= f_2g_3 + f_3g_2 \\
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\end{aligned}$$

- Ignore carries, overflows etc. for a moment
- 16 multiplications, 9 additions
- How to vectorize multiplications?

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$$

- Can easily load (f_0, f_1, f_2, f_3) and (g_0, g_1, g_2, g_3)
- Multiply, obtain $(f_0g_0, f_1g_1, f_2g_2, f_3g_3)$

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- And now what?

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- Multiply, obtain $(f_0 g_0, f_1 g_1, f_2 g_2, f_3 g_3)$
- And now what?
- Answer: Need to *shuffle* data in input and output registers
- Significant overhead, not clear that vectorization speeds up computation!

Efficient vectorization

- Most important question: Where does the parallelism come from?
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- Most important question: Where does the parallelism come from?
- Easiest answer: Consider multiple batched encryptions, decryptions, signature computations, verifications, etc.
- Often: Can exploit lower-level parallelism
- Rule of thumb: parallelize on an as high as possible level
- Vectorization is hard to do as "add-on" optimization
- Reconsider algorithms, synergie with constant-time algorithms

Going binary

- So far: considered vectors of integers
- How about arithmetic in binary fields?

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  - Computations on a transposition of data

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- Can be very fast for operations that are not natively supported (like arithmetic in binary fields)
- Active data set increases massively (e.g., $128\times$)
- For "normal" vector operations, register space is increased accordingly (e.g, 16 256-bit vector registers vs. 16 64-bit integer registers)
- For bitslicing: Need to fit more data into the same registers
- Typical consequence: more loads and stores (that easily become the performance bottleneck)

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- 256-bit vector registers `YMM0`,...,`YMM15`
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- Also supported: XOR, AND, OR on `YMM` registers (1 per cycle)
- Alternative: XOR, AND, OR on `XMM` registers (3 per cycle)
- However, don't mix `XMM` and `YMM` instruction (context-switch penalty)

Part II

Fast Lattice-Based Signatures

joint work with Tim Güneysu, Tobias Oder, and Thomas Pöppelmann

Introduction

- Consider lattice-based signature scheme proposed by Güneysu, Lyubashevsky, and Pöppelmann at CHES 2012
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- This is not a mature, well understood cryptosystem
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- Don't use it in applications, but study it!
- Implementation techniques are applicable more generally

Notation

- n is a power of 2
- p is a prime congruent to 1 modulo $2n$ (necessary for efficiency)
- $\mathcal{R}$ is the ring $\mathbb{F}_p[x]/\langle x^n + 1\rangle$
- $\mathcal{R}_k$ subset of $\mathcal{R}$ with coefficients in $[-k, k]$.

Lattice hardness assumptions

Standard lattice hardness assumption

Decisional Ring-LWE:

Given $(a_1, t_1), ..., (a_m, t_m) \in \mathcal{R} \times \mathcal{R}$. Decide whether

- $t_i = a_i s + e_i$ where $s, e_1, ..., e_m \leftarrow D_\sigma$ and $a_i \xleftarrow{\$} \mathcal{R}$ (D_σ denotes a Gaussian distribution), or
- (a_i, t_i) uniformly random from $\mathcal{R} \times \mathcal{R}$.

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More "aggressive" hardness assumption

Decisional Compact Knapsack Problem (DCKP):
Given $(a, t) \in \mathcal{R} \times \mathcal{R}$.

- Decide whether $t = as_1 + s_2$ where $s_1, s_2 \overset{\$}{\leftarrow} \mathcal{R}_1$ and $a \overset{\$}{\leftarrow} \mathcal{R}$, or
- (a, t) uniformly random from $\mathcal{R} \times \mathcal{R}$.

System parameters

Parameters

- $n = 2^{\ell_1}$
- Prime p with $2n|(p-1)$
- $k = 2^{\ell_2}$ with $\sqrt{p} < k \ll p$
- "Random" $a \in \mathcal{R}$
- Hash function H to elements of $\mathcal{R}_1$ with at most 32 non-zero coefficients

Example

- $n = 512$
- $p = 8383489$ (23 bits)
- $k = 2^{14}$
- Fixed random a
- $\ldots$ more later

Key generation

Secret key

- s_1, s_2 sampled uniformly at random from $\mathcal{R}_1$

Public key

- $t = as_1 + s_2$

Signing (simplified)

Compute a signature σ on a message M as follows:

1. Generate y_1, y_2 uniformly at random from $\mathcal{R}_k$
2. Compute $c = H(ay_1 + y_2, M)$
3. Compute $z_1 = s_1c + y_1$ and $z_2 = s_2c + y_2$
4. If z_1 or $z_2 \notin \mathcal{R}_{k-32}$, goto step 1
5. Return $\sigma = (z_1, z_2, c)$

Verification (simplified)

Check signature $\sigma = (z_1, z_2, c)$ on M as follows:

1. If z_1 or $z_2 \notin \mathcal{R}_{k-32}$, reject
2. Else if $c \neq H(az_1 + z_2 - tc, M)$, reject
3. Else accept

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Correctness

$$\begin{aligned}
&az_1 + z_2 - tc \\
&= a(s_1c + y_1) + (s_2c + y_2) - (as_1 + s_2)c \\
&= as_1c + ay_1 + s_2c + y_2 - as_1c - s_2c \\
&= ay_1 + y_2
\end{aligned}$$

Software implementation, first considerations

Key generation

- Main operation: sampling random coefficients in $\{-1, 0, 1\}$
- One multiplication of fixed a by s_1

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- Expected number of signing attempts: 7
- Each attempt:
  - Sample y_1, y_2 uniformly at random from $\mathcal{R}_k$
  - Two sparse multiplications s_1c and s_2c
  - One multiplication ay_1 by constant a

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  - One multiplication $a y_1$ by constant a

Verification

- One sparse multiplication ct
- One multiplication $a z_1$ by constant a

The function H

Need to hash an arbitrary string S to an element $c = (c_0 + c_1 x + \cdots + c_{511} x^{511})$ of $\mathcal{R}_1$ with at most 32 non-zero entries

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- First apply SHA-256, truncate to 160-bit hash h
- Map h injectively to c as follows:
  - Split $(h_0, \ldots, h_{31})$, each h_i with 5 bits
  - Split each h_i into (h_{i0}, h_{it}), where h_{i0} is one bit and h_{it} is a 4-bit integer
  - h_{it} indicates which of the 16 coefficients $c_{16i}, \ldots, c_{16i+15}$ is nonzero
  - If $h_{i0} = 0$ set this coefficient to -1 else to 1

Random sampling, 1st approach

- How do we get an integer, uniformly at random from $[0, m-1]$?
- Let's say that $m-1$ has ℓ bits
- Let's say that we can get random bits (e.g., from `/dev/urandom`)

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- Problem with both 1. and 2.: `/dev/urandom` is slow

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- Combine approaches 1 and 2 as follows:
  1. Obtain $4 \cdot (528)$ random bytes from Salsa20
  2. Interpret these bytes as 528 32-bit integers
  3. Discard integers $\geq (2k+1) \cdot \lfloor 2^{32}/(2k+1) \rfloor$.
  4. Probability to discard an integer: 2^{-30}
  5. We have 16 additional integers, replace discarded integers by those
  6. If more than 16 integers are discarded, restart with step 1
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- Similar approach to sample coefficients in $\{-1, 0, 1\}$
- Only difference: Use bytes instead of 32-bit integers

Representation of elements of $\mathcal{R}$

- represent $a = \sum_{i=0}^{511} a_i X^i$ as $(a_0, \ldots, a_{511})$:

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typedef double __attribute__ ((aligned (32))) r_elem[512];
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- Use lazy reduction: product of two 22-bit numbers has 44 bits, quite some space in the 53-bit mantissa

Multiplication in $\mathcal{R}$

- Let ω be a 512th root of unity in $\mathbb{F}_p$ and $\psi^2 = \omega$
- The number-theoretic transform NTT_ω of $a = (a_0, \ldots, a_{511})$ is defined as

$$\mathsf{NTT}_\omega(a) = (A_0, \ldots, A_{511}) \text{ with } A_i = \sum_{j=0}^{511} a_j \omega^{ij}$$

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- Component-wise multiplication is trivially vectorizable

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- FFT in a finite field
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  - Same for f_1
- For $n = 512$ we have 9 levels of recursion

NTT in AVX (Part I)

- First thing to do: replace recursion by iteration
- Loop over 9 levels with 256 "butterfly transformations" each
- Butterfly on level k:
  - Pick up a_i and a_{i+2^k}
  - Multiply a_{i+2^k} by a power of ω to obtain t
  - Compute $a_{i+2^k} \leftarrow a_i - t$
  - Compute $a_i \leftarrow a_i + t$
- Easy vectorization on levels $k = 2, \dots, 8$:
  - Pick up $v_0 = a_i, a_{i+1}, a_{i+2}, a_{i+3}$ and $v_1 = a_{i+2^k}, a_{i+2^k+1}, a_{i+2^k+2}, a_{i+2^k+3}$
  - Perform all operations on v_0 and v_1
- Levels 0 and 1: More tricky: Use permutation instructions and "horizontal additions"

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- Merge 3 levels: Load $8 \cdot 4 = 32$ values, perform arithmetic, store the results
- Final performance for NTT: 4484 cycles on Ivy Bridge
- Performance for multiplication in $\mathcal{R}$: 16096 cycles
- Multiplication by constant a: 11044 cycles

Results

- Keypair generation: 31140 cycles on Intel Ivy Bridge
- Signing: 634988 cycles on average
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- Signing: 634988 cycles on average
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- Public key: 1536 bytes
- Secret key: 256 bytes
- Signature: 1184 bytes

Comparison

Software	Cycles		Sizes	
Our work	**sign:**	634988	**pk:**	1536
	verify:	45036	**sk:**	256
			sig:	1184
`mqqsig160`	**sign:**	1996	**pk:**	206112
	verify:	33220	**sk:**	401
			sig:	20
`rainbow5640`	**sign:**	53872	**pk:**	44160
	verify:	34808	**sk:**	86240
			sig:	37
`pflash1`	**sign:**	1473364	**pk:**	72124
	verify:	286168	**sk:**	5550
			sig:	37
`tts6440`	**sign:**	33728	**pk:**	57600
	verify:	49248	**sk:**	16608
			sig:	43
XMSS	**sign:**	7261100^*	**pk:**	912
($H = 20, w = 4$, AES-128)	**verify:**	556600^*	**sk:**	19
			sig:	2451

References

- Tim Güneysu, Tobias Oder, Thomas Pöppelmann, and Peter Schwabe. *Software speed records for lattice-based signatures.*, PQCrypto 2013. `http://cryptojedi.org/papers/#lattisigns`
- Software is online (public domain) at `http://cryptojedi.org/crypto/#lattisigns`

Part III

McBits: Fast code-based cryptography

joint work with Daniel J. Bernstein and Tung Chou

Public-key encryption

- Alice generates a key pair (sk, pk), publishes pk, keeps sk secret

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- Alice uses sk decrypt C

System parameters

Parameters

- Integers m, q, n, t, k, such that
  - $n \leq q = 2^m$
  - $k = n - mt$
  - $t \geq 2$

Example

- $m = 12$,
  $n = q = 4096$
  $k = 3604$
  $t = 41$

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- An $(s + a)$-bit-output hash function H

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- $A =$ Poly1305 $(a = 256)$
- $H =$ SHA-512

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Secret key

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Key generation

Public key

- Perform Gaussian elimination on H to obtain a matrix K whose left $tm \times tm$ submatrix is the identity matrix
- K is a *public* parity-check matrix for Γ
- The public key is K

Encryption

- Generate a random weight-t vector $e \in \mathbb{F}_2^n$
- Compute $w = Ke$
- Compute $H(e)$ to obtain an $(s + a)$-bit string (k_{enc}, k_{auth})
- Encrypt the message M with the stream cipher S under key k_{enc} to obtain ciphertext C
- Compute authentication tag a on C using A with key k_{auth}
- Send (a, w, C)

Decryption

- Receive (a, w, C)
- Decode w to obtain weight-t string e
- Hash e with H to obtain (k_{enc}, k_{auth})
- Verify that a is a valid authentication tag on C using A with k_{auth}
- Use S with k_{enc} to decrypt and obtain M

Software implementation, first considerations

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- Some hassle to make constant-time, but possible

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Decryption

- Decryption is mainly decoding, lots of operations $\mathbb{F}_q$
- Decryption has to run in constant time!
- Obviously, decoding of w is the interesting part

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- Let's now fix the example parameters from above $(q = 2^m = 4096, t = 41, n = q)$

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Representing elements of $\mathbb{F}_p$

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- Use 16-bit integer values (`unsigned short`)
- Addition is simply XOR (we really XOR 64 bits, but ignore most of those)
- Multiplication:
  - Use table lookups (not constant time!)
  - Use carryless multiplier, e.g., `pclmulqdq` (not available on most architectures, again ignores most of the 64×64-bit multiplication)

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  - Squaring uses the same algorithm as multiplication

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- Use bitsliced representation in 256-bit `YMM` (or 128-bit `XMM` registers)
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- Multiplication is easily constant time, but is it fast?
- How about squaring, can it be faster?

Bitsliced multiplication in $\mathbb{F}_{2^{12}}$

- Split into 12-coefficient polynomial multiplication and subsequent reduction
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$$\begin{aligned} & (a_0 + x^n a_1)(b_0 + x^n b_1) \\ = \quad & a_0 b_0 + x^n((a_0 + a_1)(b_0 + b_1) - a_0 b_0 - a_1 b_1) + x^{2n} a_1 b_1 \end{aligned}$$

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  - Refined Karatsuba:

$$\begin{aligned} & (a_0 + x^n a_1)(b_0 + x^n b_1) \\ = \quad & (1 - x^n)(a_0 b_0 - x^n a_1 b_1) + x^n (a_0 + a_1)(b_0 + b_1) \end{aligned}$$

- Refined Karatsuba uses $M_{2n} = 3M_n + 7n - 3$ instead of $M_{2n} = 3M_n + 8n - 4$ bit operations
- For details see Bernstein "Batch binary Edwards", Crypto 2009

Bitsliced performance

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- Bitsliced *addition* is much faster than non bitsliced
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- In the following: High-level algorithms that drastically reduce the number of multiplications

Root finding, the classical way

- Task: Find all t roots of a degree-t error-locator polynomial f
- Let $f = c_{41}x^{41} + c_{40} + x^{40} + \cdots + c_0$

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- Berlekamp trace algorithm: not constant time

Remember the FFT

- Evaluate a polynomial $f = c_0 + c_1 x + \cdots + c_{n-1} x^{n-1}$ at all n-th roots of unity
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  - Write polynomial f as $f_0(x^2) + x f_1(x^2)$

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- Gao, Mateer 2010: Much faster additive FFT

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- Evaluate a polynomial $f = c_0 + c_1 x + \cdots + c_{n-1}x^{n-1}$ on a size-n $\mathbb{F}_2$-linear space S
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- Evaluate f_0 and f_1 at $\alpha^2 + \alpha$, obtain $f(\alpha)$ and $f(\alpha + 1)$ with only 1 multiplication and 2 additions
- Again: apply the idea recursively

Gao-Mateer for syndrome computation

- Application in decoding: much smaller degree of f
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  - Obtain results as subset sums of $c\beta_1, \dots, c\beta_{m-1}$
  - Replace $2^{m-1} - m$ multiplications by additions
- Overall count: fewer additions and *much* fewer multiplications than Horner scheme or Chien search

Syndrome computation, the classical way

- Receive n-bit input word, scale bits by Goppa constants
- Apply linear map

$$M = \begin{pmatrix} 1 & 1 & \cdots & 1 \\ \alpha_1 & \alpha_2 & \cdots & \alpha_n \\ \alpha_1^2 & \alpha_2^2 & \cdots & \alpha_n^2 \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_1^{2t-1} & \alpha_2^{2t-1} & \cdots & \alpha_n^{2t-1} \end{pmatrix}$$

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- Can precompute matrix mapping bits to syndrome
- Similar to encryption, but input does not have weight t
- Needs to run in constant time!

Another look at syndrome computation

Look at the syndrome-computation map again:

$$M = \begin{pmatrix} 1 & 1 & \cdots & 1 \\ \alpha_1 & \alpha_2 & \cdots & \alpha_n \\ \alpha_1^2 & \alpha_2^2 & \cdots & \alpha_n^2 \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_1^{2t-1} & \alpha_2^{2t-1} & \cdots & \alpha_n^{2t-1} \end{pmatrix}$$

Consider the linear map $M^\intercal$:

$$\begin{pmatrix} 1 & \alpha_1 & \cdots & \alpha_1^{2t-1} \\ 1 & \alpha_2 & \cdots & \alpha_2^{2t-1} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & \alpha_n & \cdots & \alpha_n^{2t-1} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \\ \vdots \\ v_t \end{pmatrix} = \begin{pmatrix} v_1 + v_2\alpha_1 + \cdots + v_t\alpha_1^{2t-1} \\ v_1 + v_2\alpha_2 + \cdots + v_t\alpha_2^{2t-1} \\ \vdots \\ v_1 + v_2\alpha_n + \cdots + v_t\alpha_n^{2t-1} \end{pmatrix} = \begin{pmatrix} f(\alpha_1) \\ f(\alpha_2) \\ \vdots \\ f(\alpha_n) \end{pmatrix}$$

- This transposed linear map is actually doing multipoint evaluation
- Syndrome computation is a transposed multipoint evaluation

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Example: An addition chain for 79

$$\begin{tikzcd}
1 \arrow[r, bend left] \arrow[r] \arrow[r, bend right] \arrow[rrrrr, bend left=40] & 3 \arrow[r, bend left] \arrow[r, bend right] \arrow[rrr, bend left=35] & 6 \arrow[r, bend left] \arrow[r, bend right] & 12 \arrow[r, bend left] \arrow[r] \arrow[r, bend right] & 39 \arrow[r, bend left] \arrow[r, bend right] & 79
\end{tikzcd}$$

Transposing linear algorithms

- A linear algorithm computes a linear map
- Allowed operations: add or multiply by a constant

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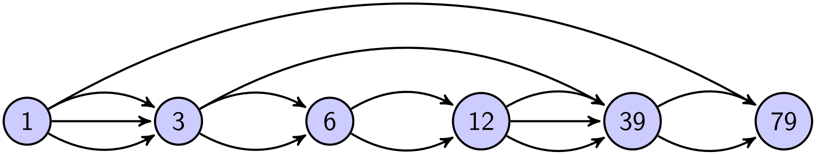
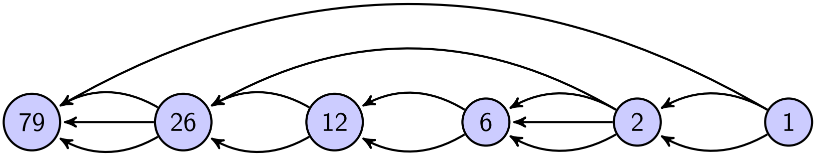


By reversing the edges, we get another addition chain for 79:



A larger example

- A linear map: $a_0, a_1 \to a_0b_0, a_0b_1 + a_1b_0, a_1b_1$

$$\begin{tikzcd}
\mathsf{in}_1 = a_0 \arrow[rr, "b_0"] \arrow[dr] & & a_0b_0 \arrow[r] \arrow[d] & \mathsf{out}_1 = a_0b_0 \\
& a_0 + a_1 \arrow[r, "b_0 + b_1"] & \mathsf{out}_2 = a_0b_1 + a_1b_0 & \\
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- Reversing the edges: $c_0, c_1, c_2 \to b_0c_0 + b_1c_1, b_0c_1 + b_1c_2$

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\mathsf{out}_1 = b_0c_0 + b_1c_1 & & c_0 + c_1 \arrow[ll, "b_0"'] & \mathsf{in}_1 = c_0 \arrow[l] \\
& (b_0 + b_1)c_1 \arrow[ul] \arrow[dl] & \mathsf{in}_2 = c_1 \arrow[l, "b_0 + b_1"'] \arrow[u] \arrow[d] & \\
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What did we just do?

- The original linear map:

$$\begin{pmatrix} a_0b_0 \\ a_0b_1 + a_1b_0 \\ a_1b_1 \end{pmatrix} = \begin{pmatrix} b_0 & 0 \\ b_1 & b_0 \\ 0 & b_1 \end{pmatrix} \begin{pmatrix} a_0 \\ a_1 \end{pmatrix}$$

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- This is called the *transposition principle*
- Preserves number of multiplications
- References: Fiduccia 1972, Bordewijk 1956, Lupanov 1956

Transposing the additive FFT

The naive approach

- Idea: Compute syndrome by transposing the additive FFT
- Start with additive FFT program (sequence of additions and constant multiplications)
- Convert to directed acyclic graph (rename variables to remove cycles)
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  - Can use better register allocators, but the program is still huge

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A better approach

- Analyze structure of additive FFT A: B, A_1, A_2, C
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- Analyze structure of additive FFT A: B, A_1, A_2, C
- A_1, A_2 are recursive calls
- Transposition has structure C^T, A_2^T, A_1^T, B^T
- Use recursive calls to reduce code size

Secret permutations

- FFT evaluates f at elements in *standard order*
- We need output in a secret order
- Same problem for input of transposed FFT
- Similar problem during key generation (secret random permutation)

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A *sorting network* sorts an array S of elements by using a sequence of *comparators*.

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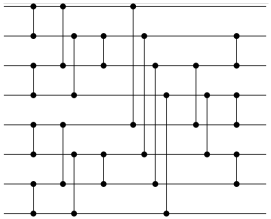
- Efficient sorting network: Batcher sort (Batcher, 1968)



Batcher sorting network for sorting 8 elements
http://en.wikipedia.org/wiki/Batcher%27s_sort

Permuting by sorting

Example

Computing b_3, b_2, b_1 from b_1, b_2, b_3 can be done by sorting the key-value pairs $(3, b_1), (2, b_2), (1, b_3)$ the output is $(1, b_3), (2, b_2), (3, b_1)$

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$$y \leftarrow b[i] \oplus b[j]; \quad y \leftarrow cy; \quad b[i] \leftarrow b[i] \oplus y; \quad b[j] \leftarrow b[j] \oplus y;$$

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- Possibly better than Batcher sort: Beneš permutation network (work in progress)

Results

Throughput cycles on Ivy Bridge

- Input secret permutation: 8622
- Syndrome computation: 20846
- Berlekamp-Massey: 7714
- Root finding: 14794
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- Total: **60493**

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- These are amortized cycle counts across 256 parallel computations
- All computations with full timing-attack protection!

Comparison

Public-key decryption speeds from eBATS

- `ntruees787ep1`: 700512 cycles
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Diffie-Hellman shared-secret speeds from eBATS

- `gls254`: 77468 cycles
- `kumfp127g` 116944 cycles
- `curve25519`: 182632 cycles

More results

CFS code-based signatures

- Signature scheme introduced by Courtois, Finiasz, and Sendrier in 2001
- Verification is very fast
- Previous speed for signing: $\approx 4.2 \cdot 10^9$ cycles on Intel Westmere (at 80 bits of security, no timing-attack protection)
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  - This is latency, no batching required

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- Estimates for 120 bits of security: ≈ 100 times slower signing, ≈ 500 MB public key

References

- Daniel J. Bernstein, Tung Chou, and Peter Schwabe. *McBits: fast constant-time code-based cryptography.*, CHES 2013. `http://cryptojedi.org/papers/#mcbits`
- Software will be online (public domain), for example, at `http://cryptojedi.org/crypto/#mcbits`